REMARKS

Amendments to the Claims

Claims 2 and 15 are amended herein.

Amendments to the Specification

The Specification was objected to as failing to provide proper antecedent basis for the claimed subject matter. The Examiner stated that there were typographical errors in Paragraph [0042], line 6 of the Specification and, specifically, that "the source regions 235 and drain regions 240" should read "the drain regions 235 and the source regions 240." Applicant has herein amended Paragraph [0042] of the Specification as suggested by the Examiner. Applicant respectfully contends that no new matter has been added by the correction of these typographical errors and notes that elements 235 and 240 are labeled as drain and source, respectively, in Figure 2A.

Applicant has also amended Paragraphs [0023] and [0047] herein to correct typographical errors. Applicant respectfully contends that no new matter has been added by the correction of these typographical errors.

Applicant therefore respectfully requests that the Examiner approve the amendments to the Specification.

Claim Objections

Claims 2 and 15 were objected to due to informalities. Specifically, the Examiner requested for claim 2 that the phrase "wherein forming a first and/or second mask layer further comprises forming a first and/or second mask layer with a photoresist" be changed to "wherein forming a first and second mask layer further comprises forming at least one of the first and second mask layer with a photoresist" to clarify scope of the claim. The Examiner also requested for claim 15 that the phrase "wherein removing the first and/or second mask layer further comprises stripping the first and/or second mask layer" be changed to "wherein removing the first and second mask layer further comprises stripping at least one of the first and second mask layer" to clarify scope of the claim. Applicant has amended the claims as suggested by the Examiner and therefore respectfully requests that the Examiner approve the amendments to claims 2 and 15.

Claim Rejections Under 35 U.S.C. § 112

Claim 17 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Applicant respectfully traverses the rejection.

The Examiner stated, in regard to claim 17, that the "[l]imitation 'patterning the first mask layer to additionally expose a portion of the layer of dielectric layer over the drain region and patterning the second mask layer to expose a portion of the layer of polysilicon over the drain region' is not supported by specification or figures."

Claim 17, recites, "wherein patterning the first and second mask layers further comprises patterning the first mask layer to additionally expose a portion of the layer of dielectric over the drain region and patterning the second mask layer to expose a portion of the layer of polysilicon over the drain region." Applicant respectfully maintains that claim 17 recites the patterning the second mask layer to expose a portion of the layer of polysilicon over the drain region and that this is supported, at least, by Paragraph [0010], Line 3; Paragraph [0013], Line 1; Paragraph [0014, Line 2; Paragraph [0047], Line 9; Paragraph [0049], Line 2; Paragraph [0060], Line 3; Paragraph [0021], Line 6; and Paragraph [0043], Line 7 of the Present Application. In particular, Paragraph [0010], Line 3 states "[e]mbodiments of the present invention are formed utilizing a wet etch process that has a high selectivity, allowing the deposition and etching of polysilicon local interconnects to source and drain regions of array transistors," and Paragraph [0043], Line 7 states "[i]t is noted that trenches for the source regions 240 and contact holes for the drain regions 235 may be formed either together or separately using one or more separate mask and etch steps," and that Paragraph [0047], Line 9 states "[i]t is also noted that the formation of bit line contacts utilizing the techniques disclosed herein. However, in forming bit line contacts, the area of dielectric and polysilicon exposed over the drain region will typically be in the form of a contact hole rather than a trench." Applicant thus contends that relevant features of claim 17 are supported and described in the specification so as to enable one skilled in the art to practice the invention.

Applicant therefore respectfully requests that the rejection of claim 17 under 35 U.S.C. § 112, first paragraph, be withdrawn in that the claim is supported by the specification and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-6 and 8-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim (U.S. Patent No. 6,001,685) in view of Wu et al. (U.S. Patent No. 6,309,975) and Applicant's Admitted Prior Art. Applicant respectfully traverses this rejection and feels that claims 1-6 and 8-17 are allowable for the following reasons.

Applicant continues to respectfully maintain that Kim teaches a method of making a self-aligned contact plug and coupled contact pad to a source that masks a dielectric layer and removes a portion from over source regions and drain regions and sequentially deposits, masks and etches layers of differing conductive material to form conductive plug contacts to the source and drain regions of differing heights and top widths. Applicant therefore respectfully maintains that Kim refers to the formation of conductive plugs of differing heights and thus does not disclose or suggest forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon.

In addition, Applicant respectfully maintains that the process of Kim patterns its mask layer so that the remaining mask material covers the polysilicon that is form the contact plug and protects it from being etched, unlike Applicant's claimed invention, where the mask layer exposes the polysilicon that is to form the local interconnect. Further, Applicant also maintains that the multiple masks and etchings of Kim to produce the multiple heights and contact plug top widths would not be operative with the ion implant and etch process of Wu et al. that etches away the silicon containing layer.

The Applicant thus submits that the method of forming a contact plug of Kim does not correspond to Applicant's method of forming a trench shaped local interconnect and that Kim's method of patterning its mask layers and etchings also does not correspond to the Applicant's method of patterning and etching. *See, e.g.*, Kim, Figure 6A-6I, Column 5, line 66 to Column 7, line 32.

Applicant also continues to maintain that Wu et al. discloses a method for masking and ion implanting layers of silicon based materials so that they can be selectively etched to preferentially remove the non-implanted portion. Applicant has also carefully reviewed Wu et al. and has found no mention of forming a trench shaped local interconnect by forming a trench shaped region in a dielectric layer, depositing a layer of polysilicon, masking the layer of polysilicon, selectively ion implanting the masked layer of polysilicon so that it can be selectively etched to preferentially remove the non-implanted portion, thereby forming the

source interconnect in the trench shaped region. Applicant therefore respectfully maintains that Wu et al. also does not teach or suggest Applicant's method of forming a trench shaped local interconnect. *See, e.g.*, Wu et al., Column 10, line 51 to Column 27, line 20.

Therefore combining the elements of Kim with Wu et al. does not teach or suggest a forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. In particular, combining the etch process of Wu et al. would not allow the second mask of Figure 6C of Kim to produce the structure of Figure 6D; the ion implant and etch process of Wu et al. would remove the desired contact plugs 32' and 32'' and leave the undesired polysilicon of the layer. Applicant contends that the ion implant and etch process of Wu et al. is also not motivation for one skilled in the art to replace mask element 33 of Figure 6C. Applicant therefore respectfully submits that Kim and Wu et al. do not teach or suggest all elements of the Applicant's claimed invention, either alone or in combination.

In regards to the Applicant's Admitted Prior Art (the APA) of Figure 1B and Paragraph [0023] of the Specification, Applicant respectfully maintains that Paragraph [0023] discloses a method of making a local interconnects and contact plugs utilizing a standard process second mask and low selectivity dry etch. As such, the Applicant respectfully maintains that the APA of Figure 1B and Paragraph [0023] of the Specification also does not teach or suggest Applicant's method of forming a trench shaped local interconnect, second mask layer, ion implant, and wet etch. *See, e.g.*, Present Application, Paragraph [0023], Lines 9-22. Therefore combining the elements of Kim and Wu et al. with the APA of Figure 1B and Paragraph [0023] of the Specification does not teach or suggest a forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. Applicant therefore respectfully submits that Kim, Wu et al. and the APA of Figure 1B and Paragraph [0023] of the Specification do not teach or suggest all elements of the Applicant's claimed invention, either alone or in combination.

In regards to the Examiner's citation of page 5 of the Applicant's Response of August 17, 2005 in rejecting claim 3, Applicant respectfully notes that the cited page responds to the Examiner's rejection of claim 3 under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has carefully reviewed page 5 of the Applicant's Response of August

17, 2005 and has found no admissions to the prior art therein, and maintains that page 5 only states that "claim 3 states that the first and second mask layers are to be patterned to remove undesired portions of the first and second mask layers with the same pattern and that such would be apparent to one skilled in the art." Applicant respectfully notes that statements contending that the disclosed material would be understood when read by those skilled in the art do not constitute admissions to that material being prior art, only that it would be understood by one skilled in the art.

Applicant's claim 1, recites, in part, "removing a portion of the exposed portion of the layer of dielectric material to form a trench shaped region and expose the source region," and "forming a layer of polysilicon overlying the layer of dielectric material and trench shaped region that is in contact with the exposed source region; forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the trench shaped region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region." As detailed above, Applicant submits that Kim, Wu et al., and the APA fail to teach or suggest such a method. As such, Kim, Wu et al., and the APA fail to teach or suggest all elements of independent claim 1. The Applicant therefore maintains that claim 1 is thus allowable over Kim, Wu et al., and the APA, either alone or in combination.

Applicant respectfully contends that claim 1 has been shown to be patentably distinct from the cited reference. As claims 2-6 and 8-17 depend from and further define claim 1, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-6 and 8-17.

Claims 1-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jenq et al. (U.S. Patent No. 6,159,788) in view of Wu et al. (U.S. Patent No. 6,309,975) and Applicant's Admitted Prior Art. Applicant respectfully traverses this rejection and feels that claims 1-15 are allowable for the following reasons.

Applicant respectfully notes that claim 7 is cancelled and is therefore not pending herein.

In regards to claims 1-6 and 8-15, Applicant continues to respectfully maintain that Jenq et al. teaches a method of making an electrode for a DRAM charge storage capacitor that sequentially deposits, masks and etches a layers of conductive material to form an electrode for a DRAM charge storage capacitor that is in contact with a source/drain region and not the formation of a local interconnect. Applicant therefore respectfully maintains that Jenq et al. does not disclose or suggest forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. The Applicant thus submits that the method of forming an electrode for a DRAM charge storage capacitor of Jenq et al. does not correspond to Applicant's method of forming a trench shaped local interconnect. *See, e.g.*, Jenq et al., Figures 4 and 5; and Column 6, lines 30-64.

In addition, Applicant respectfully maintains that the process of Jenq et al. patterns its mask layer so that the remaining mask material covers the polysilicon that is form the electrode of the DRAM charge storage capacitor and protects it from being etched, unlike Applicant's claimed invention, where the second mask layer exposes the polysilicon that is to form the local interconnect.

The Applicant thus submits that the method of forming an electrode of a DRAM charge storage capacitor of Jenq et al. does not correspond to Applicant's method of forming a trench shaped local interconnect and that Jenq et al.'s method of patterning its mask layer and etching also does not correspond to the Applicant's method of patterning and etching.

Applicant maintains, as stated above, that Wu et al. discloses a method for masking and ion implanting layers of silicon based materials so that they can be selectively etched to preferentially remove the non-implanted portion and does not disclose or suggest forming a trench shaped local interconnect by forming a trench shaped region in a dielectric layer, depositing a layer of polysilicon, masking, selectively ion implanting, and then selectively etching to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region. Applicant therefore respectfully maintains that Wu et al. also does not teach or suggest Applicant's method of forming a trench shaped local interconnect. *See, e.g.*, Wu et al., Column 10, line 51 to Column 27, line 20.

Therefore combining the elements of Jenq et al. with Wu et al. does not teach or suggest a forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. In particular, combining the etch

process of Wu et al. would not allow the mask of Figure 4 of Jenq et al. to produce the structure of Figure 5; the ion implant and etch process of Wu et al. would remove the desired DRAM electrode 44 and leave the undesired polysilicon of the layer. Applicant contends that the ion implant and etch process of Wu et al. is also not motivation for one skilled in the art to replace mask element of Jenq et al. Applicant therefore respectfully submits that Jenq et al. and Wu et al. do not teach or suggest all elements of the Applicant's claimed invention, either alone or in combination.

In regards to the Applicant's Admitted Prior Art (the APA) of Figure 1B and Paragraph [0023] of the Specification, Applicant respectfully maintains that Paragraph [0023] discloses a method of making a local interconnects and contact plugs utilizing a standard process second mask and low selectivity dry etch. As such, the Applicant respectfully maintains that the APA of Figure 1B and Paragraph [0023] of the Specification also does not teach or suggest Applicant's method of forming a trench shaped local interconnect, second mask layer, ion implant, and wet etch. *See, e.g.*, Present Application, Paragraph [0023], Lines 9-22. Therefore combining the elements of Jenq et al. and Wu et al. with the APA of Figure 1B and Paragraph [0023] of the Specification does not teach or suggest a forming a local interconnect by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon. Applicant therefore respectfully submits that Kim, Wu et al. and the APA of Figure 1B and Paragraph [0023] of the Specification do not teach or suggest all elements of the Applicant's claimed invention, either alone or in combination.

Applicant's claim 1, recites, in part, "removing a portion of the exposed portion of the layer of dielectric material to form a trench shaped region and expose the source region," and "forming a layer of polysilicon overlying the layer of dielectric material and trench shaped region that is in contact with the exposed source region; forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the trench shaped region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region." As detailed above, Applicant submits that Jenq et al., Wu et al., and the APA each fail to teach or suggest such a method. As such, Jenq et al., Wu et al., and the APA fail to teach or suggest all elements of independent

claim 1. The Applicant therefore maintains that claim 1 is thus allowable over Jenq et al., Wu et al., and the APA, either alone or in combination.

Applicant respectfully contends that claim 1 has been shown to be patentably distinct from the cited reference. Claim 7 has been cancelled. As claims 2-6 and 8-15 depend from and further define claim 1, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-6 and 8-15.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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